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Design of Low power 4-Bit CMOS Baugh- Wooley multiplier in DSM Technology

[1]G.Ramchander [2] P.Thirupathi [3] K.Harikrishna [4]Dayadi Lakshmaiah, laxmanrecw@gmail.com
[123]Assistant professors in ECE Dept, CJITS Jangaon
[4] Asso.professor, CJITS, Jangaon,TS.INDIA

*Abstract:-**A New Power 4-bit Baugh woolly multiplier is presented by a circuit design. Temperature scaling was used for the implementation of multiplier .4-bit Braun multiplier was proposed by power reduction techniques which is designed by full adders. To reduce the power dissipation by maintaining computational throughput, the design uses a cmos digital circuit which is simulated at 90nm technology with 1.2v supply. By using proposed techniques, there will be reduction of power dissipation of nearly 46%, power delay product of 56% and delay 22.2% with good performance using micro wind Tool 3.1***

Keywords:-Baugh Wooley Multiplier, Full Adder, and Temperature scaling.

1. INTRODUCTION.

The increasing prominence of portable system and the need to limit power consumption in very high density ULSI chips have led to rapid and innovative developments in low power design. The need for low power design is becoming a major issue in high performance digital systems, such as micro-processor, digital signal processing and other applications. As demands for portable computing and communication are growing, the power efficient multiplier plays an important role in Very Large Scale Integration (VLSI) system design. Multiplication is one of the essential operation in many algorithm used in Digital Signal Processing (DSP). A primary requirement of high performance digital system is high speed multiplication. In many cases multiplier may be present in critical path and speed of processing is ultimately get reduced by speed of multiplication. The Multiplier algorithm is also one of the major contributors to the total power dissipation. Reducing the power dissipation is key criteria in design of multiplier. Power consumed by multipliers can be lowered at various levels of the design from algorithm to architectures to circuit [1-15].

The core of any processor is the arithmetic and logic unit (ALU). The ALU combines the addition and subtraction with other operation. The addition and subtraction of two numbers are the basic operation in all digital computers. These operations occur at the machine instruction level and are implemented using the basic logic gates in arithmetic and logic unit (ALU) subsystem of the microprocessor. The time needed to perform these operations affects the performance of processors. Multiplication is one of the important operations which requires more complex circuitry than addition/subtraction operations. Multiplications are expensive and slow operations. In many computational problems the performance is dominated by the speed at which a multiplication operation can be executed. Multipliers are complex adder arrays. Multiplication consists of three basic operations: the generation of partial product, reduction of partial products, final carry propagate summation [21]. Considering the timing constraints, dedicated multipliers hardware implementations such as array multiplier were introduced. Variable size partial product arrays are not practical for multiplier design and since a more sophisticated methods were proposed. The modified booth recoding scheme is one of the more popular implementation. The advantage of modified booth recoding algorithm is that, it reduces the number of generated partial products by half. Bit pair recoding of the multiplier derived from booth algorithm, reduces the number of summands by a factor 2. These summands can then be reduced to only two by using a relatively small number of carry save addition steps. The final product can be generated by an addition operation that uses a carry look ahead adder [19]. The partial sum adders can be rearranged in a tree like fashion, reducing both the critical path and the number of adder cells required e.g wallace tree multiplier, Dadda. Due to irregular structure, it

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is difficult to place and route during the layout of a multiplier. A decreased size of the reduction circuit eases the

II .PROPOSED WORK

For the implementation of logic expression of eq1 and eq2, the full adder was designed with the help of 10MOS transistors. NOR-I, XNOR-II, and MUX are the three modules of 1-bit full adder. By considering two inputs and one output, XNOR-I and XNOR-II modules were designed by using 4MOS transistors. For optimum operation, the MUX module is designed with the help of two MOS transistors. The implantations of full adders are shown in fig.1 to fig.4. 6MOS transistors were combined with XNOR and XOR logic. MUX logic with 2MOS transistors for optimum operation. Implementation of full adder with 10MOS transistors is shown in fig.5.

$$Sum = \left(A \bar{\oplus} B\right)C_{in} + \left(A \oplus B\right)\bar{C}_{in} \ (1)$$

$$C_{out} = \left(A \oplus B\right)C_{in} + \left(A \bar{\oplus} B\right)A \ (2)$$

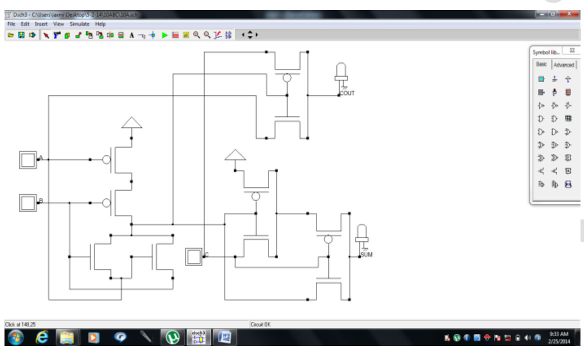

Fig. 1 Full adder10-A

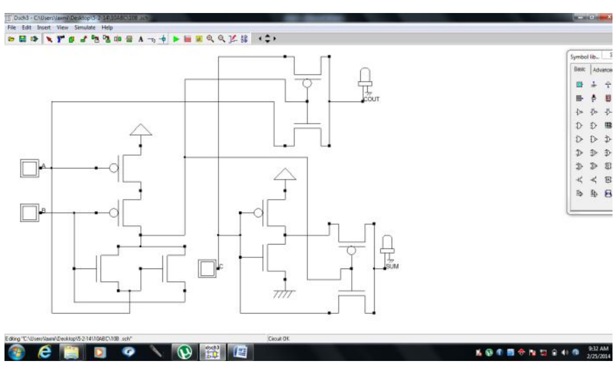

Fig. 2 Full adder10-B

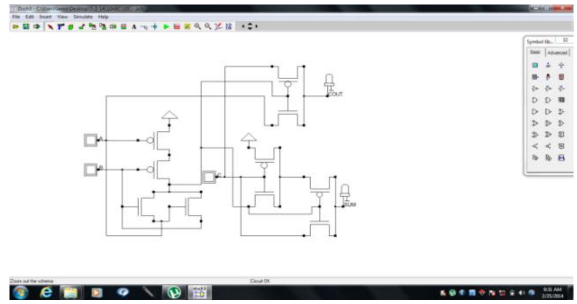

Fig. 3 Full adder10-C

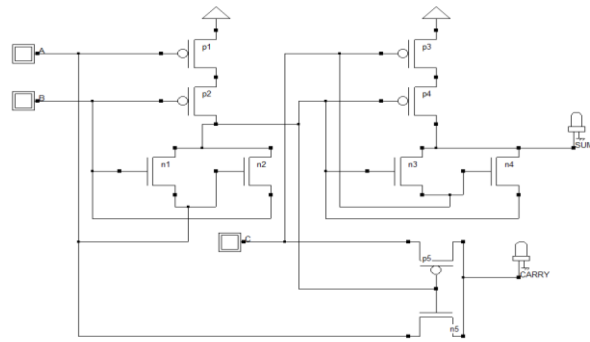

Fig. 4 Full adder10-D

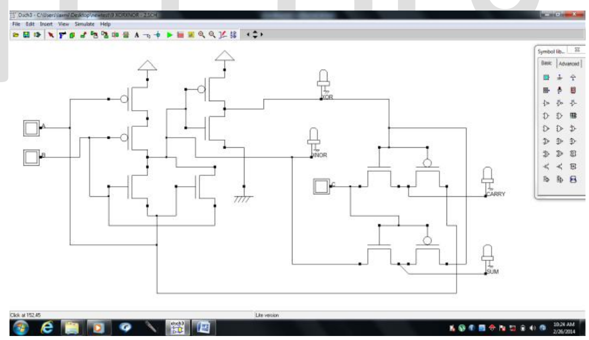

Fig. 5 Full adder10-E

III.BAUGHWOOLEY MULTIPLIER

The simplest parallel multiplier is the Baugh array. All the partial products are computed in parallel, then collected through a cascade of Carry Save Adders. The completion time is limited by the depth of the carry save array, and by the carry propagation in the adder. Note that this multiplier is only suited for positive operands. The structure of the Baughy wooley Multiplier for the signed and unsigned binary multiplication is shown in below figure.

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Baugh- Wooley Two's Compliment Signed Multiplier:

Two's Compliments is the most popular method in representing signed integers in Computer sciences. It is also an operation of negation (Converting positive to negative numbers or vice –versa) in computers which represent negative numbers using two's compliments. Its use is so wide today because it does not require the addition and subtraction circuitry to examine the signs of the operands to determine whether to add or subtract. Two's compliment and one's compliment representations are commonly used since arithmetic units are simpler to design. Fig 6 shows Two's compliment and one's compliment representations.

+N	Positive Integers	-N	Negative Integers		
			Sign & Magnitude	2's Complement	1's Complement
+0	0000	-0	1000	----	1111
+1	0001	-1	1001	1111	1110
+2	0010	-2	1010	1110	1101
+3	0011	-3	1011	1101	1100
+4	0100	-4	1100	1100	1011
+5	0101	-5	1101	1011	1010
+6	0110	-6	1110	1010	1001
+7	0111	-7	1111	1001	1000
+8	----	-8	----	1000	----

TABLE4.1: Two's compliment & one's compliment representation

Baugh-Wooley Two's compliment Signed numbers: Baugh-Wooley Two's compliment Signed multipliers is the best known algorithm for signed multiplication because it maximizes the regularity of the multiplier and allow all the partial products to have positive sign bits[3].Baugh–Wooley technique was developed to design direct multipliers for Two's compliment numbers [9].When multiplying two's compliment numbers directly,each of the partial products to be added is a signed numbers. Thus each partial product has to be sign extended to the width of the final product in order to form a correct sum by the Carry Save Adder (CSA) tree. According to Baugh-Wooley approach, an efficient method of adding extra entries to the bit matrix suggested to avoid having deal with the negatively weighted bits in the partial product matrix. In fig (6) & (7) partial product arrays of 5*5 bits Unsigned and Signed bits are shown Baugh-Wooley Two's compliment Signed numbers: Baugh-Wooley Two's compliment Signed multipliers is the best known algorithm for signed multiplication because it maximizes the regularity of the multiplier and allow all the partial products to have positive sign bits[3].

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					a_4	a_3	a_2	a_1	a_0
					x_4	x_3	x_2	x_1	x_0
					a_4x_0	a_3x_0	a_2x_0	a_1x_0	a_0x_0
				a_4x_1	a_3x_1	a_2x_1	a_1x_1	a_0x_1	
			a_4x_2	a_3x_2	a_2x_2	a_1x_2	a_0x_2		
		a_4x_3	a_3x_3	a_2x_3	a_1x_3	a_0x_3			
	a_4x_4	a_3x_4	a_2x_4	a_1x_4	a_0x_4				
p_9	p_8	p_7	p_6	p_5	p_4	p_3	p_2	p_1	p_0

FIG1 (6): 5*5 unsigned multiplications

					a_4	a_3	a_2	a_1	a_0
					x_4	x_3	x_2	x_1	x_0
					$-a_4x_0$	a_3x_0	a_2x_0	a_1x_0	a_0x_0
				$-a_4x_1$	a_3x_1	a_2x_1	a_1x_1	a_0x_1	
			$-a_4x_2$	a_3x_2	a_2x_2	a_1x_2	a_0x_2		
		$-a_4x_3$	a_3x_3	a_2x_3	a_1x_3	a_0x_3			
	a_4x_4	$-a_3x_4$	$-a_2x_4$	$-a_1x_4$	$-a_0x_4$				
p_9	p_8	p_7	p_6	p_5	p_4	p_3	p_2	p_1	p_0

FIG1 (7): 5*5 Signed Multiplication

III. PERFORMANCE AND SIMULATION RESULTS.

Baugh Wooley Multiplier Normal V_T (Normal threshold voltage) Table.1

Proposed work is implemented with the 210 MOS transistors parameters like power, area, Power Delay Product are compared with the reference paper [10].proposed results are matched with the reference paper. The architecture is optimized to less MOS Transistors compared to reference paper [10]. Where same architecture is implemented with 222 MOS Transistors The architecture consists the 15 AND gates and 12 Full Adders which is shown in the above the Fig.6. The product Boolean equation is shown in below .Where A_0 to A_3 and B_0 to B_3 are inputs and p_1 to p_7 are product of outputs.

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Table.1 Normal threshold voltage 90 nm Technology

Frequency: 200M Hz, Temperature:,26c, 90nmTechnology

Proposed 4-bit Multipliers	Power(μw)	Delay(ns)	Power Delay Product femito(10^{-15})
2011 IEEE Reference paper	220	5.510	1210
4-bit Multiplier 10-A	232	2.202	510
4-bit Multiplier 10-B	151	5.510	830
4-bit Multiplier 10-C	155	5.935	914
4-bit Multiplier 10-D	160	7.560	1200
4-bit Multiplier 10-E	74	6.090	446

Table.2, Frequency: 200M Hz, Temperature:,107c, 90nm Technology .

Proposed 4-bit Multipliers	Power(μw)	Delay(ns)	Power Delay Product femito(10^{-15})
2011 IEEE Reference paper	265	5.510	1457
4-bit Multiplier 10-A	290	2.202	638
4-bit Multiplier 10-B	205	5.510	1127

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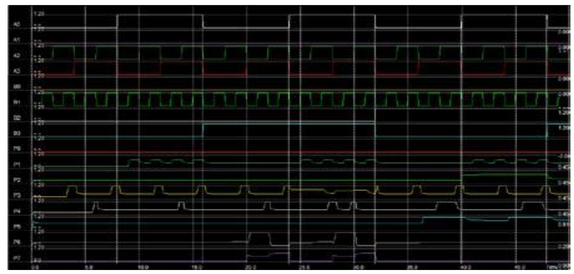
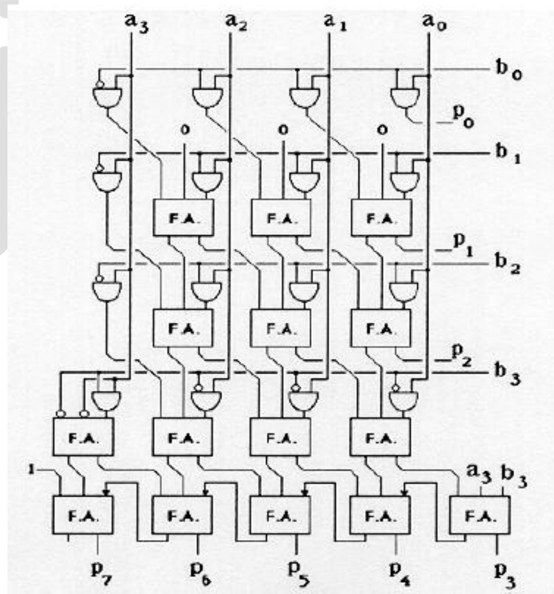
4-bit Multiplier 10-C	195	5.935	1150
4-bit Multiplier 10-D	190	7.560	1425
4-bit Multiplier 10-E	106	6.090	636



Figure(8)Baugh Wooley Multiplier 10A-Fulladder

Baugh wooley multiplier normal Vt table 1. Power, area, power delay product are the parameter which are implemented by 210MOS transistors as a proposed work to compare reference paper[10]. These proposed results were compared to reference paper[10] where architecture to be optimized that consist of 16 AND gates and 15 full adders which is shown in fig 6. Product Boolean equation is shown in below, where A0 to A3 and B0 to B3 are inputs and P1 to P7 are product of outputs. With the help of cadence micro wind software, the architecture were simulated as shown in above table1. At critical path, the MOS transistors with normal threshold voltage is used which was the proposed work. By using proposed 10-D, we observed that 4-bit Braun multiplier with power delay product is 119 femito(10^{-15}). But, by comparing with reference paper [10], it is observed that 46% of power delay product has been reduced.



Figure(9)Baugh Wooley Multiplier block diagram

As shown in the above Table.4. The proposed work of the MOS transistors with low threshold voltage was used at critical path and high threshold voltage at non critical path. It is observed that 4-bit Braun multiplier using proposed Work1 we got Power Delay Product 104 femito (10^{-15}), but comparatively to the Reference paper [10], it is 56% of power Delay Product has been reduced. Simulation results are using Micro wind Tool

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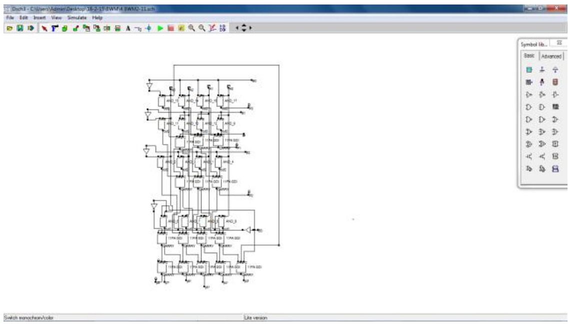

Figure (10) BAUGH WOOLY 4-Bit Multiplier using Micro wind Tool

CONCLUSION:

The present paper demonstrated the improvement in parameters v/s, power, and delay with reduction in number of transistors to implement Full adder circuits. The simulations were performed using 90nm Micro wind 3 CMOS layout CAD Tool In this paper power consumption & Power Delay Product is calculated the results are optimized power consumption of 46% and Power Delay Product is 56 % still the performance of 4-Bit CMOS Baugh Wooley Multiplier is improved by incorporating techniques which support reduced transistor implementations.

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G.Ramchander (Assistant Professor, CJITS, Janagoan) received B.E (Electronics & Communication Engineering) degree from Deccan college of Engineering and Technology,Osmania University Hyd in 2006 and M.Tech degree in Digital Communications in 2010 . Published 3 research papers in national journals & conferences. Life member of ISTE. He is having more than 8 years of experience. Subjects handled Digital signal processing, Signals and Systems, Digital image processing, Linear Integrated Circuits and Applications, Digital Logic Design, Switching Theory and Logic Design, Electronic circuits & Analysis and Radar system.

K.Harikrishna (Assistant Professor, CJITS, Janagoan) received B.Tech (Electronics & Communication Engineering) degree from VSCE Khammam in 2006 and M.Tech degree in VLSI systems design in 2011. Published 2 research papers in national journals & conferences. Life member of ISTE. He is having more than 6 years of experience. Subjects handled,Electronic devices and circuits, Linear Integrated Circuits and Applications, Digital Logic Design, Switching Theory and Logic Design, Electronic circuits & Analysis and Radar system

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P.Thirupathi (Assistant Professor, CJITS, Janagoan) received B.Tech (Electronics & Communication Engineering) degree from Pathfinder engineering college Warangal in 2013 and M.Tech degree in VLSI systems design in 2015. Published 1 research papers in national journals & conferences. He is having more than 1 years of experience. Subjects handled,Electronic devices and circuits, Electronic measuring instruments, Analog & Digitalcommunication.

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